REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Initially, applicant apologizes for the error in providing two claim 25s. The claims which are provided herein are renumbered to match the renumbering which was taken by the patent office. The undersigned apologizes for any inconvenience caused the Patent Office by this misnumbering.

The drawings stand objected to as allegedly failing to show all the claimed features. However, it is respectfully suggested that the drawings does in fact show these features. A nonvolatile memory is shown as 142. The delay element is shown as 136. Figure 1 has been amended to show that the delay element may be a phase locked loop, and also to show the graphic element.

The specification stands objected to as not including the summary of the invention section. Note, however, that Rule 73 as cited in the action is entirely voluntary. It uses the language that the application should, not must, include a summary of the invention. Intel Corp. has taken the corporate position that they prefer that applications not include a summary section. Since the provision of a summary in a patent

application is entirely voluntary, it is respectfully suggested that the objection should be withdrawn.

All of the claims stand rejected based on combinations of work individually over Coteus, Barth, Ohno. In response, each of the claims has been amended to recite additional limitations.

Claim 1 has been amended to include the limitations of claims 5, 6 and 7, and also to clarify its patentable distinctions. Specifically, amended claim 1 defines that the arbitration logic stores a number of sets of values that are used for a programmable delay element. Those sets of values are used in the delay element. The set which produces the best result is stored. This specific technique, that is storing sets of values and using the one that produces the best result, is in no way taught or suggested by Coteus, Barth and/or Ohno; no matter how combined.

Coteus discusses compensating for delays in column 7 and elsewhere. The way in which the values are obtained for the delay based compensation is described in column 11. Specifically, an amount of delay is tested, and if insufficient, it is "incremented by the predetermined phase delay amount" see column 11, lines 44-45. That is, Coteus teaches a system which increments through delays until a desired delay amount is obtained.

Barth uses a very different approach in which the delay amounts that are used for the delay lines are actually calculated based on parameters of the circuit. This is described for example in the abstract and elsewhere; specifically a response time is computed based on parameters of the circuit.

Ohno also teaches a computation technique as described column 6, lines 36-50. Specifically, the characteristics of the printed circuit board are used to calculate optimum delay information.

The present claim 1 uses a very different tactic. Specifically, different sets of delay values are stored, and each of these sets is tested. The set which works the best is obtained as the optimum delay set. Nothing in the cited prior art teaches or suggests this specific way of determining delays, and therefore it is respectfully suggested that these claims are unobvious for this reason. A number of advantages of this system can also be expected. For example, by choosing sets of delays, different optimum values which operate together can be expected. Moreover, since no calculations are necessary, this operation may be advantageous, at least in certain circumstances.

Newly added claim 47 defines another advantageous feature which is in no way taught or suggested by any of the cited prior art and specifically is not what were suggested by Coteus, Ohno or Barth. Specifically, this claim defines that the event detector detects a specified event occurring, and determines new delay values only when that specified event occurs. This feature is in no way taught or suggested by the cited prior art. The cited prior art teach nothing about calculating or determining new delay values only when the specified event occurs.

Claim 48 define an additional aspect whereby the new values are obtained in response to a change in system configuration. Once again, this is in no way taught or suggested by the cited prior art.

Claim 13 has been amended to include the limitations of claims 14 and 15 therein. Specifically, these claims now define similar subject matter to that discussed above with respect to claim 47 and specifically that the arbitration logic controls the delay element to determine new delay values only when a specified event occurs. Claims 16 and 17 define these specified events as being respectively a hardware change or a system crash. None of this is in any way taught or suggested by the

cited prior art, as described above. Claim 18 defines the multiple sets as described above with respect to claim 1.

Claim 22 has been amended to include the limitations of claim 26 therein and began defines the system event, which is in no way taught or suggested by the cited prior art.

Claim 33 has been amended to recite the multiple sets of delay values, which again is nowhere taught or suggested by the cited prior art. Claim 37 has been amended to emphasize this feature, and began defines the event the system event causing new delay values, and otherwise not.

Claim 42 has been amended to include the limitations of claim 44 therein. According to claim 42 as amended, the delay values cause the signal to have a specified relationship with one another and that specified relationship is unsynchronized. Nothing in the prior art teaches or suggests such a specified relationship which is not synchronized. Again, this goes completely against the teaching in the art which defines all of the values being synchronized, not on synchronized.

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

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Respectfully submitted,

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